

LOW VOLTAGE QUAD BUS BUFFERS (3-STATE) WITH 5V TOLERANT INPUTS

- HIGH SPEED: $t_{PD}=4.4ns$ (TYP.) at $V_{CC} = 3.3V$
- 5V TOLERANT INPUTS
- POWER-DOWN PROTECTION ON INPUTS
- INPUT VOLTAGE LEVEL:
 $V_{IL} = 0.8V$, $V_{IH} = 2V$ at $V_{CC} = 3V$
- LOW POWER DISSIPATION:
 $I_{CC} = 2 \mu A$ (MAX.) at $T_A=25^\circ C$
- LOW NOISE:
 $V_{OLP} = 0.3V$ (TYP.) at $V_{CC} = 3.3V$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $I_{OHL} = I_{OL} = 4 mA$ (MIN) at $V_{CC} = 3V$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(OPR) = 2V$ to $3.6V$ (1.2V Data Retention)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 125
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74LVX125 is a low voltage CMOS QUAD BUS BUFFERS fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. It is ideal for low power, battery operated and low noise 3.3V applications.



Table 1: Order Codes

PACKAGE	T & R
SOP	74LVX125MTR
TSSOP	74LVX125TTR

This device requires the 3-STATE control input \overline{G} to be set high to place the output into the high impedance state.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V. It combines high speed performance with the true CMOS low power consumption.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Figure 1: Pin Connection And IEC Logic Symbols

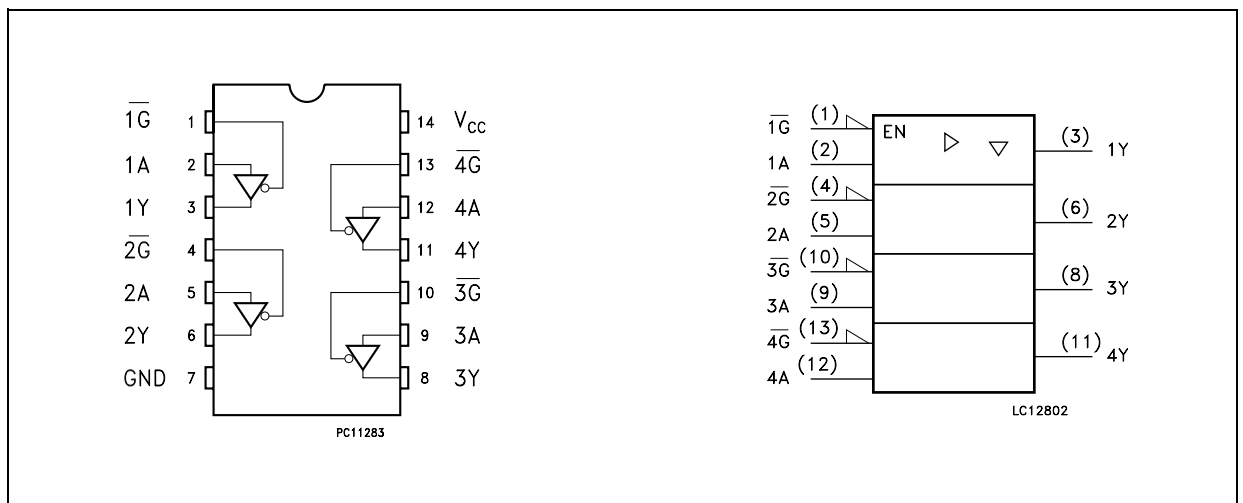


Figure 2: Input Equivalent Circuit

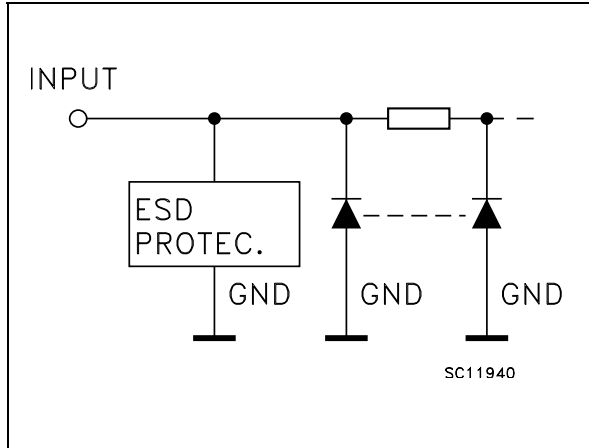


Table 2: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
1, 4, 10, 13	1G to 4G	Output Enable Inputs
2, 5, 9, 12	1A to 4A	Data Inputs
3, 6, 8, 11	1Y to 4Y	Data Outputs
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

Table 3: Truth Table

A	\bar{G}	Y
X	H	Z
L	L	L
H	L	H

X : Don't Care
Z : High Impedance

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage (note 1)	2 to 3.6	V
V _I	Input Voltage	0 to 5.5	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 2) (V _{CC} = 3V)	0 to 100	ns/V

1) Truth Table guaranteed: 1.2V to 3.6V

2) V_{IN} from 0.8V to 2.0V

Table 6: DC Specifications

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		3.0		2.0			2.0		2.0		
		3.6		2.4			2.4		2.4		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		3.0				0.8		0.8		0.8	
		3.6				0.8		0.8		0.8	
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9		
		3.0	I _O =-4 mA	2.58			2.48		2.4		
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1	
		3.0	I _O =4 mA			0.36		0.44		0.55	
I _{OZ}	High Impedance Output Leakage Current	3.6	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.25		± 2.5		± 5	μA
I _I	Input Leakage Current	3.6	V _I = 5.5V or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	3.6	V _I = V _{CC} or GND			2		20		20	μA

Table 7: Dynamic Switching Characteristics

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	3.3	C _L = 50 pF		0.3	0.5					V
V _{OLV}				-0.5	-0.3						
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	3.3		2.0							
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	3.3				0.8					

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 3.3V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 3.3V. Inputs under test switching: 3.3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

Table 8: AC Electrical Characteristics (Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)	C_L (pF)	$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t_{PLH} t_{PHL}	Propagation Delay Time	2.7	15		5.8	10.1	1.0	13.5	1.0	14.5	ns
		2.7	50		8.3	13.6	1.0	17.0	1.0	18.0	
		3.3 ^(*)	15		4.4	6.2	1.0	8.5	1.0	9.5	
		3.3 ^(*)	50		6.9	9.7	1.0	12.0	1.0	13.0	
t_{PZL} t_{PZH}	Output Enable Time	2.7	15		5.3	9.3	1.0	12.5	1.0	13.5	ns
		2.7	50		7.8	12.8	1.0	16.0	1.0	17.0	
		3.3 ^(*)	15		4.0	5.6	1.0	7.5	1.0	8.5	
		3.3 ^(*)	50		6.5	9.1	1.0	11.0	1.0	12.0	
t_{PLZ} t_{PHZ}	Output Disable Time	2.7	50		10.0	15.7	1.0	19.0	1.0	20.0	ns
		3.3 ^(*)	50		8.3	11.2	1.0	13.0	1.0	14.0	
t_{OSLH} t_{OSHL}	Output to Output Skew Time (note 1,2)	2.7	50		0.5	1.0		1.5		1.5	ns
		3.3 ^(*)	50		0.5	1.0		1.5		1.5	

1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW

2) Parameter guaranteed by design

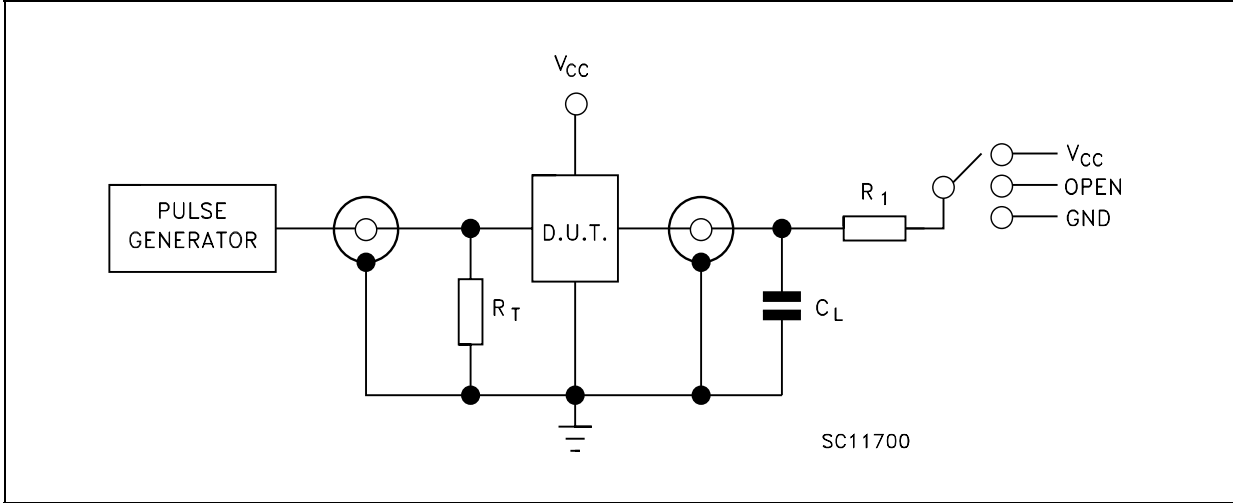
(*) Voltage range is $3.3\text{V} \pm 0.3\text{V}$

Table 9: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value						Unit	
		V_{CC} (V)		$T_A = 25^\circ\text{C}$			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C_{IN}	Input Capacitance	3.3			4	10		10		10	pF
C_{OUT}	Output Capacitance	3.3			6						pF
C_{PD}	Power Dissipation Capacitance (note 1)	3.3			14						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4$ (per circuit)

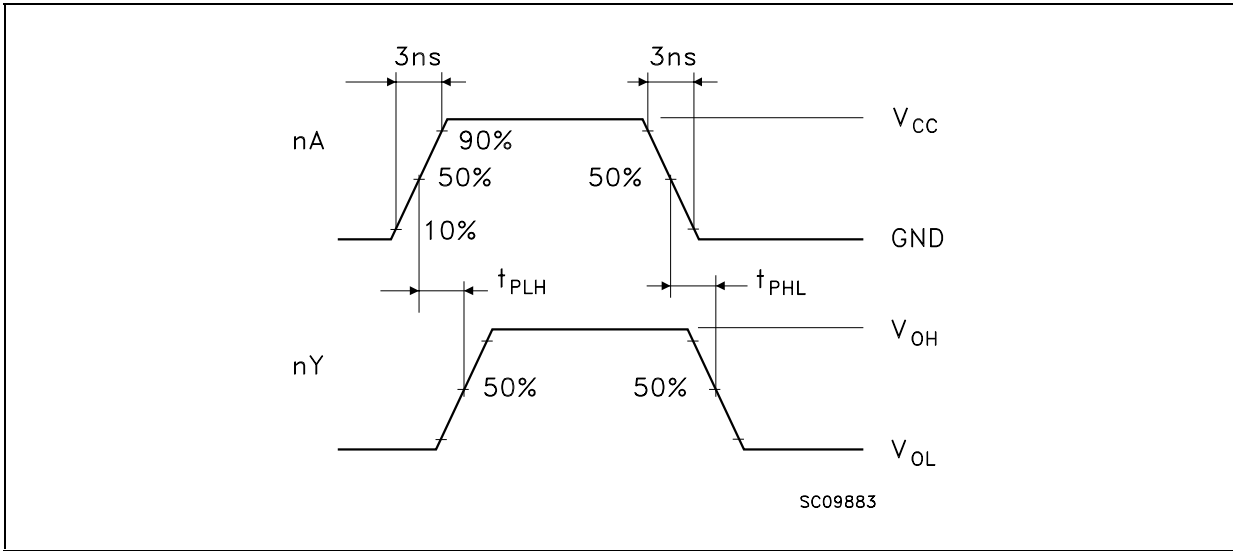
Figure 3: Test Circuit



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

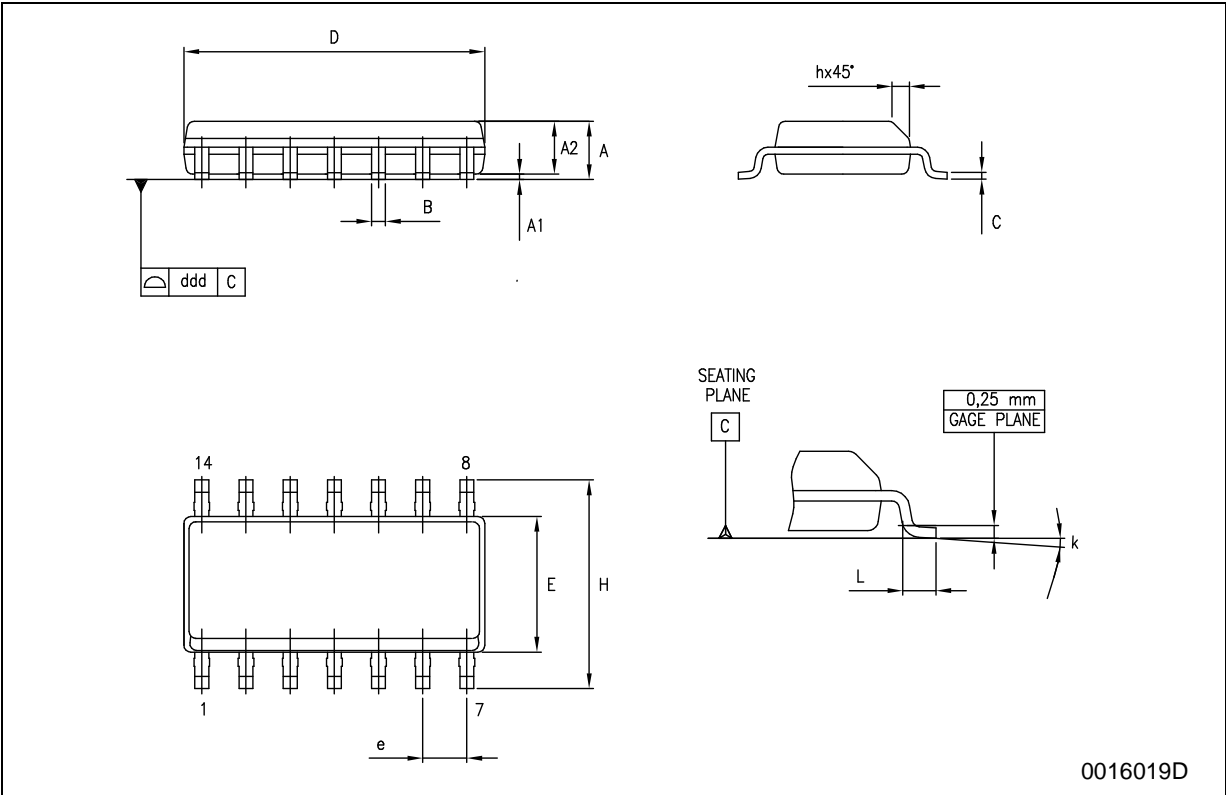
$C_L = 15/50\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = R_1 = 1\text{K}\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 4: Waveform - Propagation Delays ($f=1\text{MHz}$; 50% duty cycle)



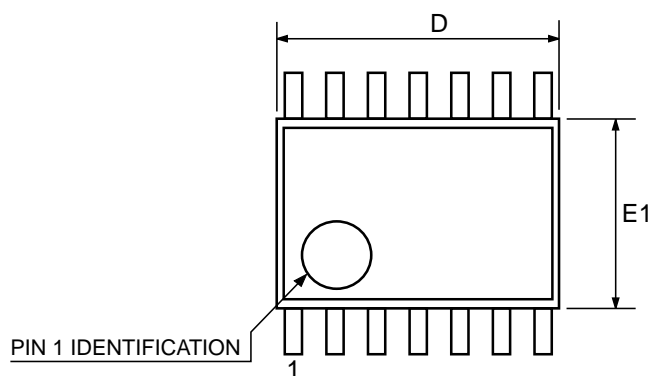
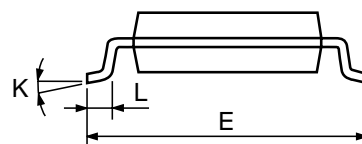
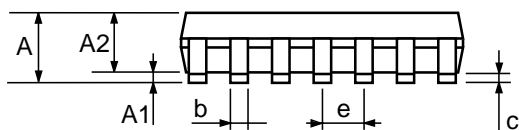
SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.1		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	8.55		8.75	0.337		0.344
E	3.8		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.2	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.4		1.27	0.016		0.050
k	0°		8°	0°		8°
ddd			0.100			0.004



TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0080337D

Tape & Reel SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.4		6.6	0.252		0.260
Bo	9		9.2	0.354		0.362
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Tape & Reel TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Table 10: Revision History

Date	Revision	Description of Changes
27-Aug-2004	3	Ordering Codes Revision - pag. 1.

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